UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/334,354	06/16/1999	JUNJI TAJIME	P/2054-107	5240

7590	08/18/2004

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EXAMINER
LEE, RICHARD J

ART UNIT	PAPER NUMBER
2613	26

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

	Application No.		Applicant(s)
Office Action Summary	09/334,354		TAJIME ET AL.
	Examiner		Art Unit
	Richard Lee		2613

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>07 June 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

1.   The request filed on June 7, 2004 for a Request for Continued Examination (RCE) is

acceptable and a RCE has been established. An action on the RCE follows.

2.   The Examiner wants to point out that the applicant's arguments from the amendment

filed April 29, 2004 have been noted and considered but are deemed moot in view of the

following new grounds of rejections.

3.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making
> and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it
> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
> contemplated by the inventor of carrying out his invention.

4.   Claims 1-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with

the written description requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed

invention. .

The Specification does not provide support for the newly amended limitations " a

memory bus that accesses said memory; a memory access width controller that controls said

quantization controller such that bit allocation is controlled in relation to a number of bits of the

memory bus that accesses said memory" as shown at claim 1, lines 9-12; "in conformity with the

number of bits ... of the memory bus that accesses said memory" as shown at claim 2, lines 4-7;

"a memory access width controller ... compression processing exceeds the number of bits of

memory bus that accesses said memory" as shown at claim 9, lines 10-19; "memory access width

controller ... in conformity with the number of bits of the memory bus that accesses said

memory, based on an occupied content of said memory" as shown at claim 10, lines 2-5; "the

memory access width controller ... the allocated number of bits is made equal to or less than the number of bits of the memory bus that accesses said memory by subtracting a predetermined number of bits from the allocated bits of coded data of said compression processing block or by increasing the number of allocated bits by the predetermined number of bits" as shown at claim 12, lines 2-12; "controlling said number of coded bits sot that said number of coded bits is in conformity with the number of bits of a memory bus that accesses a memory when said detected number of coded bits exceeds the number of bits of a memory bus that accesses said memory" as shown at claim 17, lines 4-7.

As understood by the Examiner, the present invention involves a moving picture decoding apparatus for decoding compressed image data. Part of the decoding apparatus includes a memory access width control section 110 for applying control to quantizer control section 109 so that a number of coded data bits is conformed to be equal to or less than the number of bits of the memory access unit (see pages 4-5 of the Specification). The Specification, at page 5, describes how "in the case that the allocated number of bits is less than the number of bits M1 of a memory access unit, and a frame memory has enough capacity, allocation of the number of bits of the coded data can be also increased" and "the memory access width control section (110 of Fig. 1) applies control of an access width of the frame memory to the quantization control section". The Specification, at page 8, describes how "The access width control section 110 applies control to the quantization control section 109 using information of the frame memory 106 so that the information content for a single or a plurality of memory compression processing units or for every control unit of the memory compression process is conformed to be equal to or less than the number of bits of a memory access unit.".

The Examiner has thoroughly reviewed the Specification and believes that the above cited

passages from the disclosure are the most relevant description pertaining to the newly claimed

limitations. But, it is clear from these passages that there is no adequate support for a memory

bus and control of the number of coded bits so that the number of coded bits is in conformity

with the number of bits of a memory bus that accesses a memory when the detected number of

coded bits exceeds the number of bits of a memory bus that accesses the memory as claimed.

Further, the Specification lacks any description of the comparison of a number of bits of a

memory bus with the number of coded bits; allocation of bits control in relation to a number of

bits of the memory bus; and controlling of a number of bits to be equal to or less than the number

of bits of the memory bus in the case that the number of bits for every control unit of

compression processing exceeds the number of bits of memory bus that accesses the memory as

currently claimed.

5.   Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing

to particularly point out and distinctly claim the subject matter which applicant regards as the

invention.

        At claim 2, lines 4-5, the phrase "is in conformity with the number of bits of memory that

accesses said memory" as claimed is vague and indefinite in that it is unclear what is being

claimed.

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7.   Claims 1-14 and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohira

et al of record (6,208,689).

The Examiner wants to point out that the newly amended limitations to the claims that

constitute as new matter (see above paragraph (4)) have not been considered in the following art

rejections.

Ohira et al discloses a method and apparatus for digital image decoding as shown in

Figures 18, 19, 24, 29, 30, 49-53, and the same moving picture decoding method and apparatus

as claimed in claims 1-14 and 16-18, comprising the same compressor (i.e., 107a of Figures 18

and 24, 112a of Figure 49, see 107b of Figures 29 and 30) that compresses a decoded image and

stores the resulting compressed image in a memory (i.e., 103 of Figures 18 and 49); an expander

(i.e., see 108, 109 of Figure 18; 113a, 114a of Figure 49) that expands a compressed image

stored in the memory; a quantization controller (see Figures 18, 19, 24, 29, 30, 50-52, column

13, line 61 to column 14, line 64, column 15, line 56 to column 16, line 45, column 24, line 37 to

column 25, line 12) that controls how quantization is performed in the compressor; a memory

access width controller (i.e., as provided by compression rate judging section 106 of Figure 18

since compression rate judging section 106 provides the rate of compression in connection with

the storage capacity, i.e. number of bits of the memory 103, and bit allocation control to the

quantization controller is being provided within 107a of Figures 18, 24, 107b of Figures 29, 39,

and 112a of Figures 49 and 50, see Figures 18, 24, 29, 30, 49-52, column 13, lines 16-44, column

14, lines 3-64, column 17, line 33 to column 19, line 13) that controls the quantization controller

such that bit allocation is controlled in relation to the number of bits of a memory access unit of

the memory, the memory access width controller controls the quantization controller such that a

number of coded bits of the image processed in the compressor for every control unit of

compression processing is in conformity with the number of bits of the memory access unit of

the memory in the case that the coded number of bits exceeds the number of bits of the memory

access unit of the memory, the memory access width controller conducts control using

information included in the compressed stream, the memory access width controller applies

control to the quantization controller such that when an allocated number of bits of coded data of

a compression block exceeds the number of bits of the memory access unit of the memory or is

less than the number of bits of the memory access unit of the memory, the allocated number of

bits is made equal to or less than the number of bits of the memory access unit of the memory by

subtracting a predetermined number of bits from the allocated bits of coded data of the

compression processing block or by increasing the number of allocated bits by the predetermined

number of bits, whereby the coded data is enabled to be extracted from the memory with one

access occurrence (i.e., data in the compressing section 107a of Figure 18 are compressed based

upon the compression rate information 157 from the compression rate judging section 106, the

compression rate judging section selects a compression mode from among a plurality of

compression modes based upon the rate of compression, thereby providing the increase/decrease

in the number of bits allocated and providing the rate of compression in connection with the

memory, i.e. number of bits, of the memory 103, and bit allocation control to the quantization

controller is being provided within 107a of Figures 18, 24, 107b of Figures 29, 39, and 112a of

Figures 49 and 50, and see column 13, lines 16-44, column 14, lines 3-64, column 17, line 33 to

column 19, line 13); the quantization controller controls quantization performed by the

compressor based on access width information from the memory access width controller such

that a number of bits processed in the compressor for every control unit of compression

processing is equal to or less than the number of bits of the memory access unit of the memory in

the case that the number of bits for every control unit of compression processing exceeds the

number of bits of memory access unit of the memory (i.e., compression rate judging section 106

provides the rate of compression in connection with the storage capacity, i.e. number of bits of

the memory 103, and the compressing section 107a or 107b which includes quantization control

based on access width information compresses the data based upon the compressed rate

information provided by compression rate judging section, see Figures 18, 24, 29, 30, 49-52,

column 13, lines 16-44, column 14, lines 3-64, column 17, line 33 to column 19, line 13);

wherein the compressor and the expander conduct compression and expansion, respectively, in

accordance with a pixel difference prediction encoding system (see 107a of Figure 24, 107b of

Figures 29 and 30, column 4); wherein the quantization controller (see 107b of Figures 29 and

30, 703a of Figures 50 and 51) controls quantization by preparing a plurality of quantizers (i.e.,

121a-d of Figures 29 and 30; 703a of Figure 51) having quantization characteristics different

from each other and a plurality of quantization characteristic tables, a quantization characteristic

table (see 700 of Figure 50) being shared by the plurality of quantizers; wherein the compressor

and expander conduct compression and expansion, respectively, in accordance with an

orthogonal translation encoding system (see column 4, column 9, lines 1-13); the compressor

controls quantization characteristics used for quantizing the decoded image, based on control by

the quantization controller (see Figures 29, 30, 50, 51); detecting a number of coded bits for

every control unit of compression processing (i.e., 107a of Figures 18 and 24), and controlling

the number of coded bits so that the number of coded bits is in conformity with the number of

bits of a memory access unit of a memory (i.e., 103 of Figure 18) when the detected number of

coded bits exceeds the number of bits of a memory access unit of the memory, wherein the step

of controlling uses information from an external compressed data stream (see column 13, lines

16-44, column 13, line 61 to column 14, line 64, and 106 of Figure 18).

8.   Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohira et al as

applied to claims 1-14 and 16-18 in the above paragraph (7), and further in view of Nakajima et

al of record (6,243,421).

        Ohira et al discloses substantially the same moving picture decoding method and

apparatus as above, but does not particularly disclose the compressor comprising a subtracter, a

quantizer, an encoder, an inverse quantizer, an adder and a predictor, a prediction error obtained

in the subtracter by subtraction operation between the decoded image and a predicted value from

the predictor is supplied to the quantizer, under control of the quantization controller, the

quantizer quantizes the prediction error and supplies the quantized result to the encoder and the

inverse quantizer, the encoder encodes an output from the quantizer and outputs the encoded

result to the memory, and inverse quantizer and local decoding are conducted in the inverse

quantization, the adder and the predictor, as claimed in claim 15. However, Nakajima et al

discloses an apparatus for decoding coded video data with reduced memory size as shown in

Figures 2 and 3, and teaches the conventional compression means comprising a subtracter (20 of

Figure 3), a quantizer (21 of Figure 3), an encoder (22 of Figure 3), an inverse quantizer (25 of

Figure 3), an adder (23 of Figure 3) and a predictor (24 of Figure 3), a prediction error (i.e.,

output of 20 of Figure 3) obtained in the subtracter by subtraction operation between the decoded

image and a predicted value from the predictor is supplied to the quantizer, under control of the

quantization controller, the quantizer (i.e., 21 of Figure 3) quantizes the prediction error and

supplies the quantized result to the encoder (22 of Figure 3) and the inverse quantizer (25 of

Figure 3), the encoder encodes an output from the quantizer and outputs the encoded result to the

memory (i.e., 6 of Figure 2), and inverse quantization and local decoding are constructed in the

inverse quantization, the adder, and the predictor (see Figure 3). Therefore, it would have been

obvious to one of ordinary skill in the art, having the Ohira et al and Nakajima et al references in

front of him/her and the general knowledge of video compression systems, would have had no

difficulty in providing the compression means as shown in Figure 3 of Nakajima et al including

all the components as claimed in place of the compression system 107a of Figure 18 of Ohira et

al for the same well known video compression with quantization control purposes as claimed.

9.   Any response to this action should be mailed to:

> Commissioner of Patents and Trademarks
> Washington, D.C. 20231

or faxed to:

> (703) 872-9314, (for formal communications intended for entry)

> (for informal or draft communications, please label "PROPOSED" or "DRAFT")

> Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal
> Drive, Arlington. VA., Sixth Floor (Receptionist).

10.   Any inquiry concerning this communication or earlier communications from the
examiner should be directed to Richard Lee whose telephone number is (703) 308-6612. The
Examiner can normally be reached on Monday to Friday from 8:00 a.m. to 5:30 p.m, with
alternate Fridays off.

        Any inquiry of a general nature or relating to the status of this application should be
directed to the Group customer service whose telephone number is (703) 306-0377.

RICHARD LEE
PRIMARY EXAMINER

Richard Lee/rl

8/11/04